REMARKS

Applicant respectfully requests reconsideration of this application. Claims 1-3 and 5-30 are pending. Claims 1, 3, 8, 10, 11, 18, 21, 23, 25, and 26 have been amended. Claims 2 and 22 have been cancelled. No claims have been added. Therefore, claims 1, 3, 5-21, and 23-30 are now presented for examination.

Claim Rejection under 35 U.S.C. §102 and §103

Levine, et al.

The Examiner rejected claims 1, 2, 4-17, 21, 22, and 24-30 under 35 U.S.C. 102 (e) as being anticipated by U.S Patent 6,134,710 of Levine, et al. ("Levine").

The Examiner had further rejected claims 3, 18-20, and 23 under 35 U.S.C. 103 (a) as being unpatentable over Levine as applied to claim 2, 10, and 22.

For the sake of convenience in evaluating the amendments to the claims and the arguments presented here, the three independent claims, as amended, are presented as follows:

1. An event monitoring component for dynamic optimization comprising:

   an event monitor hardware component to selectively capture a plurality of profiles of one or more microarchitecture events occurring in the execution of an application by a microprocessor based upon configuration information supplied by a software component;

   a profile buffer to store the plurality of captured profiles of the one or more microarchitecture events;

   an interface through which the software component provides the configuration information to direct the operation of the event monitor; and

one or more monitor control vectors, the monitor control vectors storing the configuration information provided by the software component, wherein *each monitor control vector includes a handler field to hold a pointer to a handler routine to process the profiles of the microarchitecture event.*

10. A microprocessor, comprising:

an execution pipeline;

one or more event monitor hardware components coupled to the execution pipeline to selectively monitor one or more microarchitecture events in the execution of a program and to capture a plurality of event profiles;

one or more monitor control vectors to store configuration information provided by a software component in connection with the operation of the one or more event monitor hardware components, *each monitor control vector including a handler field to contain a pointer to a handler routine for the microarchitecture event*; and

a profile buffer to store captured microarchitecture event profiles.

21. A method comprising:

receiving configuration information from a software component directing the monitoring of one or more microarchitecture events connected with the operation of a microprocessor in executing an application, wherein receiving the configuration information includes receiving information regarding the setting of one or more monitor control vectors, *each monitor control vector including a handler field to contain a pointer to a handler routine for processing of captured profiles of the microarchitecture event*;

monitoring the one or more microarchitecture events using an event monitor in hardware and capturing profiles of the one or more microarchitecture events;

storing the captured event profiles in a profile buffer; and

making the profiles of the event available to the software component for optimization processing.

(emphasis added) With regard to these claims, the Applicant respectfully submits the following:

Elements of the Claims – The claims have been modified to clarify the hybrid system operation in connection with the hardware and software elements. Claim 1 provides for an event monitoring component for dynamic optimization, which includes an "event monitoring hardware component" for selectively capturing a plurality of profiles for microarchitecture events occurring I the execution of an application "based upon configuration information supplied by a software component". Claims 10 and 21 also include elements regarding the monitoring by hardware components and the provision of configuration by software, as shown above.

Further, the claims address the use of handler routines. For example, claim 1 provides that each monitor control vector includes a handler field to hold a pointer to a handler routine to process the profiles of the microarchitecture event.

The Operation of Levine – In addition to any other differences, Applicant respectfully submits that Levine does not contain the elements of the claims with regard to a vector including a pointer to a handler routine.

With regard to the elements of the claims, Applicant notes the provisions of the Office Action regarding claims 3, 18, and 23, which were rejected under 35 USC §103

citing to Levine alone. It is submitted that such elements are not obvious and that Levine is not a sufficient reference for rejection of such elements.

With regard to claim 3, the Office Action admits that Levine does not expressly disclose a handler field containing a pointer to handler routine. The Office Action states that "the system of Levine inherently includes such a pointer. The address of the handler routine must be known in order to service the interrupt and process the profiles of the event (see, for example, column 10, lines 63 to column 11, line 3)." The Office Action applies the same argument to claims 18 and 23. The Applicant respectfully traverses this assertion.

There is no evidence that Levine contemplates a handler field to hold a pointer to handling routine. The fact that Levine discusses a system in which certain collected data that is processed does not inherently lead to the elements of the claims presented herein. The data could be handled in many different ways, and is not necessarily or inherently connected with the software instructions provided in a vector.

Levine specifically illustrates the control mechanism for the monitoring processes, and there is no teaching or suggestion of a handler field to hold a pointer to a handler routine. Levine indicates that monitor mode control registers control the operation of monitor elements. These are illustrated as elements 110 and 120 of Figure 2.

> The performance monitor 80 has, typically, two monitor mode control registers, MMCR0 110 and MMCR1 120. It also has special purpose registers (SPRs) that are used as performance monitoring counters: PMC0 130, PMC1 140, PMC2 150, through PMC7 160. The monitor mode control registers and the performance monitor counters are normally 32 bit in length, but may be any reasonable length. *The events to be monitored by the performance monitor 80 are selected by the event*

> *detection and control logic 170 under control of MMCR0 110 and MMCR1 120. ... The monitor mode control registers MMCR0 110 and MMCR1 120 control the operation of the performance monitor counters PMC0 130, PMC1 140, PMC2 150, through PMC7 160.* FIG. 3 illustrates a typical configuration of MMCR0 110 and MMCR1 120 for control of PMC0 130, PMC1 140, PMC2 150, through PMC7 160.

(Levine, col. 7, line 59 through col. 8, line 13)

Referring then to Figure 3, the fields provided in these control registers are illustrated. Levine then provides a very detailed explanation of the elements of the control registers, indicating that the registers "are configured into a number of control fields that control events to be counted, enable performance monitoring interrupts and control condition to enable counting." (Levine, col. 8, lines 19-22) The interrupts are further explained, with an explanation that that when enabled interrupts are generated when the most significant bit of the selected counter transitions from a logical 0 to a logical 1. (Levine, col. 8, lines 25-27)

Thus, Levine has described a system in which certain registers are to control events that are to be monitored and are to enable specific interrupt operations, thereby providing a certain set of operations. There is no teaching or suggestion the existence of handler fields to hold or contain pointers to handler routines, and, since Levine describes in depth a system that does use such features, the elements cannot be said to be inherent in Levine.

For at least the above reasons, it is respectfully submitted that Levine does not contain the elements of the independent claims 1, 10, and 18. The remaining claims are dependent claims and, while have other distinguishing features, and allowable as being dependent on the allowable base claims.

Conclusion

Applicant respectfully submits that the rejections have been overcome by the amendment and remark, and that the claims as amended are now in condition for allowance. Accordingly, Applicant respectfully requests the rejections be withdrawn and the claims as amended be allowed.

Invitation for a Telephone Interview

The Examiner is requested to call the undersigned at (503) 439-8778 if there remains any issue with allowance of the case.

Request for an Extension of Time

The Applicant respectfully petitions for a one-month extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a). A check is enclosed to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 10/3/05

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